Chapter 10

PREPARATION OF AL/ZN3%-PVA/P-SI STRUCTURES AND INVESTIGATION OF THEIR ELECTRICAL BEHAVIOR

Yosef BADALI[1]

INTRODUCTION

Since metal-semiconductor (MS) structure has an interlayer such as insulator, polymer and ferroelectric material, MS structure converts to the MIS, MPS and MFS structure, respectively [1-6]. Such an interlayer does not only obviate the reaction between metal and semiconductor but also improves the performance and quality of the structure as a diode or solar cell devices. The thickness and formation quality of the insulating layer between metal and semiconductor are important parameters which affect the main electrical values. In resent, polymer based MS structure have been attracting for researches that are alternative to traditional insulator layer such as SiO_2 and SnO_2 due to their low cost, easy grown, flexibility and good performance [7-9]. In addition, the traditional interfacial insulator or oxide layer with low dielectric constant cannot completely passivation the active dangling bounds at the semiconductor surface. On the other hand, it is anown that the use of high dielectric material can be reduced the series resistance (*Rs*), surface states (*Nss*), leakage reverse current (*IR*) and increase of shunt resistance (*Rsh*), rectifying rate (*RR=IF/IR*) at enough high forward and reverse biased, and barrier height (*FB*) [10-14].

In many scientific studies, various materials have been added to the polymer matrix for use as a interfacial layer between the semiconductor and polymer to improve the electrical and dielectric properties of the MS structures [1, 15-19]. Among them, Reddy et al. [16], procreated Au/$BaTiO_3$/n-GaN structures and notified that *IR* values of Au/n-GaN structures are larger and the RR values are lower than that of the Au/$BaTiO_3$/n-GaN structures. This is proof that the MIS structure performs better than the MS structure. Çetinkaya et al. [20] fabricated Au/

[1] Dr, Gazi University, bedeli.yusuf@gmail.com

CONCLUSION

In this work the $Zn_{3\%}$-PVA interfacial layer with 0, 10, 20, 30, 50 nm thickness was deposited on the silicon wafer via electro-spinning method to obtained Al/$Zn_{3\%}$-PVA/p-Si MPS type SBD structures. The main electrical parameters of prepared structures such as reverse saturation current (*I0*), barrier height (*FB0*), rectifying rate (*RR*), ideality factor (*n*), series and shunt resistances (*Rs* and *Rsh*) and surface states (*Nss*) were found from the *I-V* characteristics. Experimental results show that these parameters are strong functions of interlayer thickness and observed a good linear relation between *FB0* and n as *FB0* =(-0.129*n*+0.96) eV. The prepared all Al/$Zn_{3\%}$-PVA/p-Si MPS samples appear to have good diode properties. In particular, the shunt resistances of the samples with $Zn_{3\%}$-PVA interfacial layer are very high, indicating that they have a unique structure for diode applications. Specially when the obtained results were compared in respect of interfacial layer thickness, the MS structure with 20 nm and 30 nm interface layer thickness show the best performance as a diode.

Keywords: MPS structures, Thickness dependent, Rectifying rate, Surface states, Series resistance

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